SIGMA-DELTA MODULATOR USING A PASSIVE FILTER

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of signal processing and more specifically to a sigma-delta modulator using a passive filter.

BACKGROUND OF THE INVENTION

Sigma-delta modulation typically involves using active filters to perform integrator functions. Active filters, however, may include active components such as transistors and operational amplifiers that may consume a significant amount of power. Additionally, depending on the active components of active filters may require the sigma-delta modulation to run at limited speeds.

SUMMARY OF THE INVENTION

In accordance with the present invention, disadvantages and problems associated with previous techniques for sigma-delta modulation may be reduced or eliminated.

According to one embodiment a sigma-delta modulator includes a discrete time circuit that receives a digital feedback signal and an input signal, where the input signal includes information and one or more analog input currents. The discrete time circuit converts the digital feedback signal into an analog feedback signal during a first discrete time and sums the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals. A continuous time circuit includes passive elements, is coupled to the discrete time circuit, and operates to filter the one or more summed signals using a first-order filter and a second-order filter in order to generate one or more filtered signals. A quantizer is coupled to the continuous time circuit and generates the digital signal using the one or more filtered signals, where the digital signal comprising the information.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be that a sigma-delta modulator does not require active components, which may allow the sigma-delta modulator to run at low power and low voltage. Another technical advantage of one embodiment may be that the sigma-delta modulator may be run at speeds unconstrained by components, which may allow the sigma-delta modulator to yield a higher resolution while maintaining low power consumption.

Certain embodiments of the invention may include none, some, or all of the above technical advantages. One or more other technical advantages may be readily apparent to one skilled in the art from the figures, descriptions, and claims included herein.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram of one embodiment of a sigma-delta modulator using a passive filter in accordance with the present invention; and

FIGURE 2 is a circuit diagram of one embodiment of the sigma-delta modulator of FIGURE 1 that may be used in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention and its advantages are best understood by referring to FIGURES 1 and 2 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIGURE 1 is a block diagram of one embodiment of a sigma-delta modulator 10 using a passive filter in accordance with the present invention. In general, sigma-delta modulator 10 performs the analog to digital conversion of a signal by sampling and quantizing an analog signal using a discrete time circuit and a continuous time circuit that each include passive elements. According to the illustrated embodiment, sigma-delta modulator 10 includes a transconductance stage 12, a discrete time stage 14, a continuous time stage 16, and a quantizer 16 coupled as shown in FIGURE 1.

Transconductance stage 12 receives an input voltage signal and converts it to an input current signal. According to one embodiment, transconductance stage 12 comprises at least one transconductor that receives an analog signal comprising a positive voltage signal and a negative voltage signal. The positive voltage signal and the negative voltage signal may each be converted to a current signal with a current value proportional to the voltage amplitude of the corresponding signal. According to another embodiment, transconductance stage 12 may comprise a resistor that may be used if the input analog voltage signal requires a highly linear response. Any other configuration suitable for performing transconductance of an input voltage signal may be used without departing from the scope of the invention.

Discrete time stage 14 includes a discrete time circuit that performs discrete time operations. According to one embodiment, discrete time stage 14 comprises a plurality of switches and a feedback capacitor that perform operations at discrete times. For example, at a first discrete time the feedback capacitor is charged to a reference voltage, and at a second discrete time the feedback capacitor generates a current and reference voltage through summing node *B* in order for discrete time circuit 14 to sum a feedback signal and the input signal at summing node *B*.

To perform discrete time operations, discrete time stage 14 receives control signals and a digital feedback signal. As will be more particularly described with reference to FIGURE 2, the control signals may comprise at least two discrete time signals φ_1 and φ_2. The discrete time signals φ_1 and φ_2 may activate the switches to perform the discrete time operations such as sampling the input signal, converting the digital feedback signal into an analog feedback signal, and summing the sampled input signal with the feedback signal. As another example, the discrete time circuit may generate a quantization error signal corresponding to the input analog signal by calculating the difference between the input analog signal and the analog feedback signal. Any other suitable function may be performed by the discrete time circuit of discrete time stage 14 without departing from the scope of the invention.

Continuous time stage 16 includes a continuous time circuit that may be used for filtering the quantization error signal. According to one embodiment, the continuous time circuit comprises a first order filter

and a second order filter that operate to low-pass filter a signal according to a desired response. For example, the first order filter may comprise a first capacitor that filters the quantized error signal according to a first low-pass response to yield a first filtered signal. The first capacitor may be selected such that the ratio between the capacitance of the first capacitor and the capacitance of the feedback capacitor are substantially greater than one. The second order filter may comprise a resistor and a second capacitor that filter the first filtered signal according to a second low-pass response to yield an integrated signal.

According to one embodiment, although the filtering performed by the first order filter and the second order filter may be characterized as low-pass filtering, the filters may generate an integrated signal if the filters operate at a high frequency. Continuous time stage 16 may include passive components such as resistors and capacitors in order to perform the filtering functions at high frequencies, thus enabling the sigma-delta modulator 10 to perform at high frequencies while consuming low power. Any other suitable passive components may be used to perform the continuous circuit functions without departing from the scope of the invention.

Quantizer 16 digitizes the integrated signal to yield a digital signal corresponding to the sampled input analog signal. According to the illustrated embodiment, quantizer 16 comprises a comparator that amplifies the integrated signal and compares the inputs to each other to generate a quantized signal. For example, the integrated signal may comprise two voltage signals that may be input at the comparator so that the voltage

signals may be compared to each other and yield the digital output corresponding to the sampled analog signal. Quantizer 18 may comprise any other suitable one bit analog-to-digital converter without departing from the scope of the invention.

Modifications, additions, or omissions may be made to the system without departing from the scope of the invention. For example, transconductance stage 12 may be omitted such as if an analog input signal in current mode is applied to the discrete time stage 14. As another example, continuous time stage 16 may comprise filter circuits of any other suitable order without departing from the scope of the invention. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding. "Each" as used in this document refers to each member of a set or each member of a subset of a set.

FIGURE 2 is a circuit diagram of one embodiment of the sigma-delta modulator 10 of FIGURE 1 that may be used in accordance with the present invention. In operation, sigma-delta modulator 10 receives an input analog signal and timing signals 20. According to one embodiment, timing signals 20 comprise nonoverlapping phase clock signals φ_1 and φ_2. A continuous time circuit filters signals received from a discrete time circuit to generate an integrated signal that is quantized by a comparator to yield a digital output. According to the illustrated embodiment, discrete time circuit and continuous time circuit comprise passive components that may enable sigma-delta modulator 10 to perform at high frequencies while consuming low power.

As was described with reference to FIGURE 1, a transconductance stage 12 receives an input analog voltage V_{in} and converts the input analog voltage V_{in} into a current-mode analog signal. According to the illustrated embodiment, input analog voltage V_{in} is converted to a couple of current sources, where each current source corresponds to a positive input voltage V_{inp} and a negative input voltage V_{inm}. These current sources continuously deliver a current to summing node *B*. Transconductance stage 12 may improve the linearity of sigma-delta modulator 10; however, transconductance stage 12 may be omitted and replaced by a coupling resistor if a sufficiently large analog input signal in voltage-mode is applied to sigma-delta modulator 10. Transconductance stage 12 may also be omitted if a current-mode input signal is applied directly to sigma-delta modulator 10.

At summing node *B*, the current-mode analog signals are summed according to the discrete time operation of the switches and feedback signal. According to the illustrated embodiment, feedback capacitors C_{R1} are precharged to reference voltages V_{refp} and V_{refm} according to a pulse of first discrete time signal φ_1 . Precharging feedback capacitors C_{R1}, which may result in an overall gain error, relaxes buffering speed requirements.

Feedback capacitors C_{R1} discharge a discharge current to the appropriate side of the summing node *B* according to a pulse of second discrete time signal φ_2, . For example, on the positive side of the sigma-delta modulator 10, if digital signal *Y* is high, the discharge current is summed at the minus side of summing node *B*, and if digital signal *Y* is low, the discharge current is summed at the positive side of summing node *B*. Summing

the discharge current in this fashion may result in the differential summing of the analog input signal and the digital signal *Y*, which is converted to an analog mode signal according to the discharge current.

The analog input signals (in current mode) are discretized and summed with the feedback signal at summing node *B* to yield quantization error signals according to a pulse of second discrete time signal φ_2 . The quantization error signals may be characterized as the difference between the analog input signal and a feedback signal, which in this case is the converted digital signal *Y*. Additional discrete times and additional switched circuits may be used without departing from the scope of the invention. Consequently, additional timing signals 20 may be used without departing from the scope of the invention.

According to the illustrated embodiment, the quantization error signals are filtered at continuous time stage 16 by a first order filter 24 and a second order filter 26. First order filter 24 and the second order filter 26 low-pass filter the quantization error signals If sigma-delta modulator 10 processes signals at high frequencies, first order filter 24 and second order filter 26 may operate as an integrator that integrates the quantization error signal without the use of operational amplifiers that may require a specific bandwidth and frequency of operation and power consumption as compared to a passive circuit as that illustrated.

First order filter 24 comprises a first capacitor C_1 that filters the quantization error signal to yield a first filtered signal. First capacitor C_1 may be directly

coupled to summing node *B* to low-pass filter the quantization error signal. According to one embodiment, first capacitor C_1 may be selected so that the ratio between first capacitor C_1 and feedback capacitor C_{R1} satisfies Equation (1):

$$\frac{C_1}{C_{R1}} >>> 1 \qquad (1)$$

Second order filter 26 comprises a second capacitor C_2 and a second resistor R_2 that filter the first filtered signal to yield an integrated signal. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be directly coupled to integration node *C* to filter the first filtered signal according to a low-pass response. Second capacitor C_2 and a second resistor R_2 may be selected according to a desired frequency response. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be selected so that the frequency response substantially approximates a direct current (DC) frequency response. For example, second capacitor C_2 and a second resistor R_2 may be selected according to Equation (2):

$$\frac{1_1}{R_2 C_2} \approx DC \qquad (2)$$

where *DC* is the DC frequency at which second order filter operates. A stabilizing resistor R_0 may be used to increase the stability of the continuous time circuit. Any other suitable passive components may be used at continuous time circuit and any additional or other

filtering circuits may be used without departing from the scope of the invention.

Comparator 18 is engaged during the inverse of the first discrete time signal $\overline{\varphi_1}$ to amplify the voltage of the signal present at integration node *C*. According to the illustrated embodiment, second discrete time signal φ_2 may have a delay 22 to ensure that a digital signal *Y* is available before amplifying the signal received from integration node *C*. Making available a valid digital output *Y* at the comparator before the next pulse of second discrete time signal φ_2, may allow for smoother DAC conversion. This embodiment may also reduce or eliminate high timing jitter requirements on the clock that may involved with implementing a feedback DAC.

According to the illustrated embodiment, the comparator receives a minus loop signal at the noninverting input and a positive loop signal at the inverting input. The comparator may compare the signals present at the inverting and noninverting inputs to generate digital output *Y*. It will be understood that the comparator may comprise any voltage comparator or any other device suitable for quantizing a received analog signal. Any other suitable one bit analog-to-digital (A/D) converter may be used at the comparator without departing from the scope of the invention.

Modifications, additions, or omissions may be made to the system without departing from the scope of the invention. For example, other suitable first order and second order filters may be used. Additionally, functions may be performed using any suitable logic comprising software, hardware, other logic, or any suitable combination of the preceding.

Certain embodiments of the invention may provide one or more technical advantages. A technical advantage of one embodiment may be that a sigma-delta modulator does not require active components, which may allow the sigma-delta modulator to run at low power and low voltage. Another technical advantage of one embodiment may be that the sigma-delta modulator may be run at speeds unconstrained by components, which may allow the sigma-delta modulator to yield a higher resolution while maintaining low power consumption.

Although an embodiment of the invention and its advantages are described in detail, a person skilled in the art could make various alterations, additions, and omissions without departing from the spirit and scope of the present invention as defined by the appended claims.